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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/780,360	02/12/2001	Dae Young Kim	2950-0186P	7013

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EXAMINER	
BRITT, CYNTHIA H	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 07/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/780,360	KIM ET AL.	
	Examiner	Art Unit	
	Cynthia Britt	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 January 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 November 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-30 are presented for examination.

This Office action replaces the Office Action mailed January 27, 2005.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-7 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claim 1, the phrase "...and combining the plurality of data blocks as appended into one ECC (Error Correction Code) block to perform an error correction on the basis of the ECC block;" is unclear. The examiner would like to point out that most if not all of the prior art presented teach the use of inner and outer parity in a matrix form, interleaved and stored on a storage medium. The addition of the phrase mentioned above does not seem to add any function, as the block of data appears to be in the standard format (as disclosed in the background portion of this application and also in Han U.S. Patent No. 6,378,103 Figure 8). In general, *error correction is preformed on the data based on an error correction code* not based on a block. Although the claims are interpreted in light of the specification, limitations from the specification are not read

into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). It is unclear to the examiner based on the wording of these claims that there would be any difference in the way the ECC process would function in this claim or the prior arts of record. Pages 5-7 of the current specification appear to contain the core of this disclosure, specifically the matter contained in Figure 5.

As per claims 2-7, these claims are dependent on the rejected independent claims and inherit the 35 U.S.C. 112, second paragraph issues of the independent claim and will not be further considered on the individual merits of each claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, and 8-30 are rejected under 35 U.S.C. 102(e) as being anticipated by Jeong et al. U.S. Patent No. 6,539,512.

As per claims 1 and 8, Jeong et al. teach an interleaving method for a high density recording medium in which, an intrablock interleaver interleaves received data having a predetermined error correction code within an error correction block to output intrablock-interleaved data. An interblock interleaver interleaves the intrablock-interleaved data between the error correction blocks in units of a predetermined number of the error correction blocks to output interblock-interleaved data. Figures 8 and 12 show the details of the rows being ordered sequentially and the combination of two blocks. Intersector interleaving is performed with respect to two error correction blocks. (Abstract, Figures 8 and 12, column 3 lines 14-34, column 8 lines 35-47, column 9 lines 48-64)

As per claim 9, Jeong et al. teach intrablock interleaving is performed by interleaving 16 outer parity rows with sectors by adding one outer parity row to the end of each sector, in the same way as row interleaving for a general DVD format. (Column 4 lines 31-40)

As per claim 10, Jeong et al. teach writing the rows sequentially by row number in the interleaving process. (Figure 12)

As per claim 11, Jeong et al. teach 8 to 16 modulation. (Column 4 lines 41-47)

As per claim 12, Jeong et al. teach outer parity is 16 bytes long and inner parity 10 bytes. (Figure 1)

As per claim 13, Jeong et al. teach outer parity is 16 bytes long appended on each column and inner parity 10 bytes long appended on each row. (Figure 1)

As per claim 14, Jeong et al. teach an interleaving method for a high density recording medium in which, an intrablock interleaver interleaves received data having a predetermined error correction code within an error correction block to output intrablock-interleaved data. An interblock interleaver interleaves the intrablock-interleaved data between the error correction blocks in units of a predetermined number of the error correction blocks to output interblock-interleaved data. Figures 8 and 12 show the details of the rows being ordered sequentially and the combination of two blocks. Intersector interleaving is performed with respect to two error correction blocks. (Abstract, Figures 8 and 12, column 3 lines 14-34, column 8 lines 35-47, column 9 lines 48-64)

As per claims 15 and 27, Jeong et al. teach intrablock interleaving is performed by interleaving 16 outer parity rows with sectors by adding one outer parity row to the end of each sector, in the same way as row interleaving for a general DVD format. (Column 4 lines 31-40)

As per claim 16, Jeong et al. teach 8 to 16 modulation and writing the rows sequentially by row number in the interleaving process. (Figure 12 Column 4 lines 41-47)

As per claims 17 and 18, Jeong et al. teach a modulator to modulate data that has been interblock-interleaved, using a predetermined modulation scheme (here, 8-to-16 modulation). A sync inserter inserts two 32-bit sync patterns with respect to the modulated data and outputs the resultant data to be recorded on a disc. (Column 4 lines 41-47)

As per claim 19, Jeong et al. teach outer parity is 16 bytes long appended on each column and inner parity 10 bytes long appended on each row. (Figure 1)

As per claim 20, Jeong et al. show it is inherent that merging two blocks 208 x 182 would either give you 208 x 364 or 416 x 182 (figures 4, 8 and 12)

As per claims 21, Jeong et al. teach a storage medium which uses an interleaving method (for a high density recording medium) in which, an intrablock interleaver interleaves received data having a predetermined error correction code within an error correction block to output intrablock-interleaved data. An interblock interleaver interleaves the intrablock-interleaved data between the error correction blocks in units of a predetermined number of the error correction blocks to output interblock-interleaved data. Figures 8 and 12 show the details of the rows being ordered sequentially and the combination of two blocks. Intersector interleaving is performed with respect to two error correction blocks. Intrablock interleaving is performed by interleaving 16 outer parity rows with sectors by adding one outer parity row to the end of each sector, in the same way as row interleaving for a general DVD format. (Abstract, Figures 8 and 12, column 3 lines 14-34, column 8 lines 35-47, column 9 lines 48-64)

As per claim 22, Jeong et al. teach a data unit having a data unit size of 172 x 192. (Figure 1)

As per claims 23 and 24, Jeong et al. teach a modulator to modulate data that has been interblock-interleaved, using a predetermined modulation scheme (here, 8-to-16 modulation). A sync inserter inserts two 32-bit sync patterns with respect to the

modulated data and outputs the resultant data to be recorded on a disc. (Column 4 lines 41-47)

As per claim 25, Jeong et al. teach outer parity is 16 bytes long appended on each column and inner parity 10 bytes long appended on each row. (Figure 1)

As per claims 26 and 28, Jeong et al. show it is inherent that merging two blocks 208 x 182 would either give you 208 x 364 or 416 x 182 (figures 4, 8 and 12)

As per claim 29, Jeong et al. teach writing the rows of two interleaved blocks sequentially by row number in the interleaving process. (Figure 12)

As per claim 30, Jeong et al. teach an error correction coder (ECC) error-correction codes data read from an HD-DVD and provides error-correction coded data. An error correction code used in the ECC is the same as a Reed-Solomon (208, 192, 17) code used in a general DVD. Here, 208 denotes the number of codewords, 192 denotes the size of user data within the total codewords, and 17 denotes a value obtained by adding one to the number of parities. (Figure 3 column 4 lines 20-30)

Claims 8-10, and 14-15 are rejected under 35 U.S.C. 102(e) as being anticipated by Zook U.S. Patent No. 6,052,815.

As per claims 1, 2, 8-10, and 14-15, Zook teaches using product codes (inner and outer parity) to form a matrix (data block) of data to be interleaved and stored in a storage medium. Using an error correction system for computer storage devices that

avoids the latency associated with verifying the validity and completeness of corrections to a multi-dimensional code. The validation is carried out using a cyclic redundancy check (CRC). During a write operation, it CRC redundancy symbols are computed over user data received from a host system, and after appending the CRC symbols, the data is randomized by XORing it with a pseudo random data pattern. ECC symbols are then generated over the randomized data to form row (Q) and column (P) codewords of a product code; the product code is then written to the disk. Upon readback, the product code is stored in a data buffer for decoding by a P/Q decoder. During a first pass over the Q codewords, a data CRC syndrome is generated over the uncorrected randomized data; the data CRC syndrome is stored in a data CRC register. Also during the first pass and subsequent passes, when corrections are made to the P or Q codewords the correction values are applied to an error CRC register. After processing a complete CRC codeword, the data CRC and error CRC registers are combined to generate a final CRC syndrome. The final CRC syndrome is compared to a constant to determine if the corrections to the product code are valid and complete, where the constant equals the CRC over the random data pattern. In this manner, the CRC check can be performed over the randomized data, thereby avoiding the latency associated with accessing the data buffer to derandomize the data before generating the CRC syndrome. (Figures 3A, 3B, and figure 11,column 5 line 23 through column 6 line 14, column 8 lines 22-51)

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent No. 6,378,103 Han

This patent teaches an apparatus and method for error correction in an optical disk system. An optical disk reproducing system calculates syndromes for each codeword to set an eraser flag during EFM demodulation. Error-correction-coding is performed using the eraser flag after completion of EFM-demodulation to reduce the access time for a data memory in error correction, thus reducing the time of error correction. The system includes a data memory for storing the EFM signals and the EFM-demodulated signals in the unit of an error correction block, an EFM demodulation and syndrome calculator for EFM-demodulating the EFM signals to output the EFM-demodulated signals to the data memory, and for calculating syndromes of the EFM-demodulated signals in the unit of the first codeword and outputting a flag indicating errors.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cynthia Britt whose telephone number is 571-272-3815. The examiner can normally be reached on Monday - Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 571-272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Cynthia Britt
Examiner
Art Unit 2133